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K4F4C K4H1A K4H3A K9D1 K9R2

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EP 0497596 A EP 0466166 A EP 0364818 A
JP 010093077 A US 5652156 A

(58) Field of Search
UK CL (Edition Q ) H1K KCAA KCAL KCAX KGAFX
KGAGX KHAAX KHABP KHAC KHAX
INT CL[6] H01L
online: EPODOC,WPI,JAPIO

(54) Abstract Title
**Gate electrode for a semiconductor device**

(57) A semiconductor device is provided which is capable of suppressing an increase in the layer resistance of the gate electrode and preventing an increase of the contact resistance of the gate electrode with a silicide layer.

These properties of the semiconductor device are provided by forming the gate electrode with multiple layers. The lowermost layer 23 of the gate electrode is doped with an impurity such as phosphorus, and other, upper layer(s) 24 are formed undoped. The layers 23,24 may be polysilicon, an annealing process producing large grains in the lowermost layer 23 and small grains in the upper layer(s) 24. The layers are separated by oxide 9.

Fig. 1

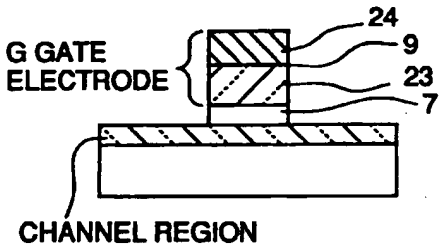


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Fig. 1

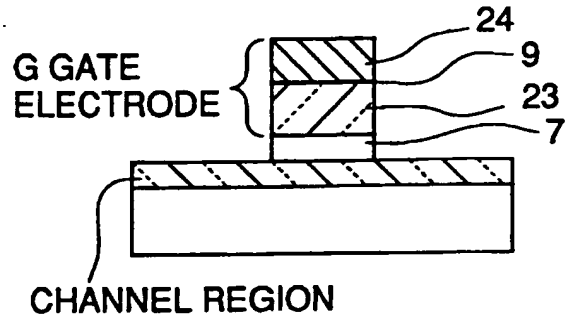



Fig. 3

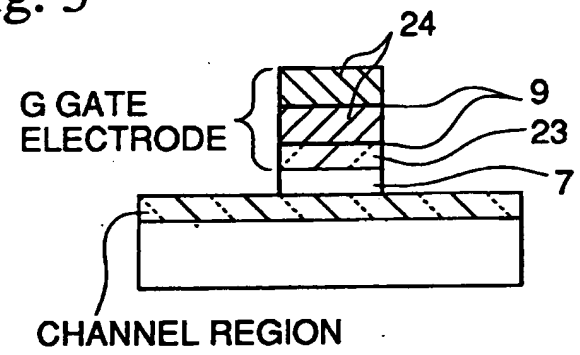



Fig. 4

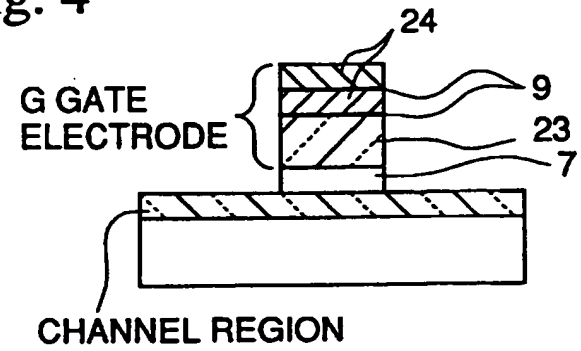



Fig. 5

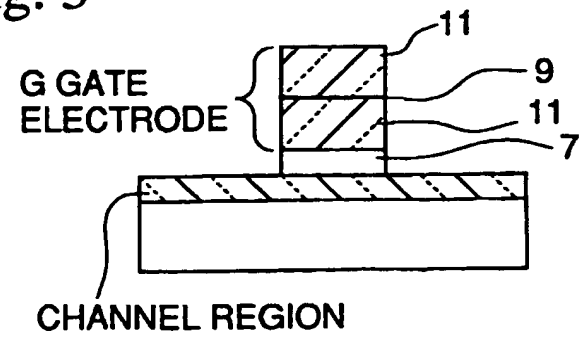


Fig. 2A

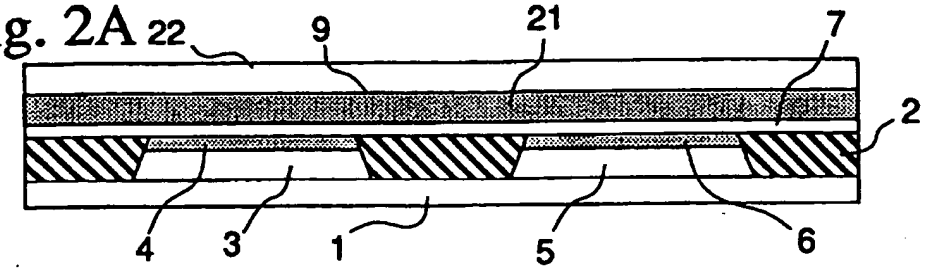



Fig. 2B

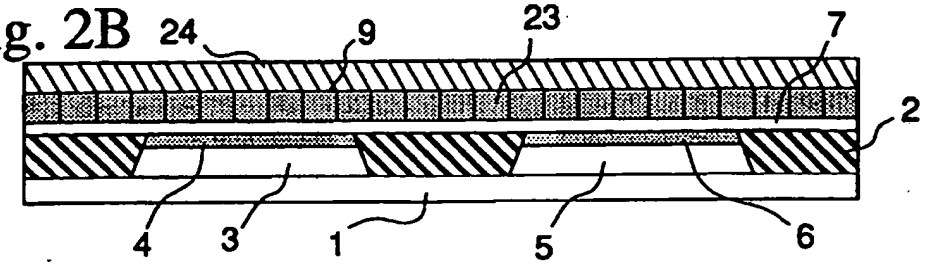



Fig. 2C

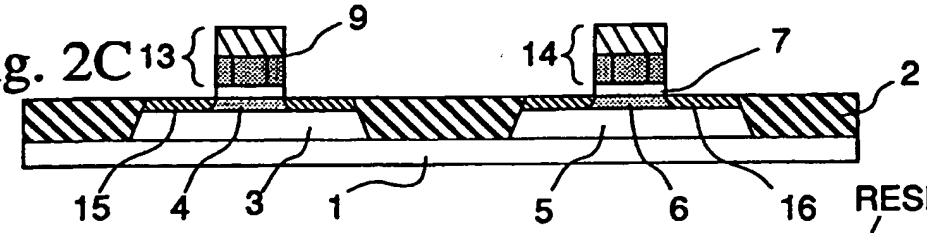



Fig. 2D

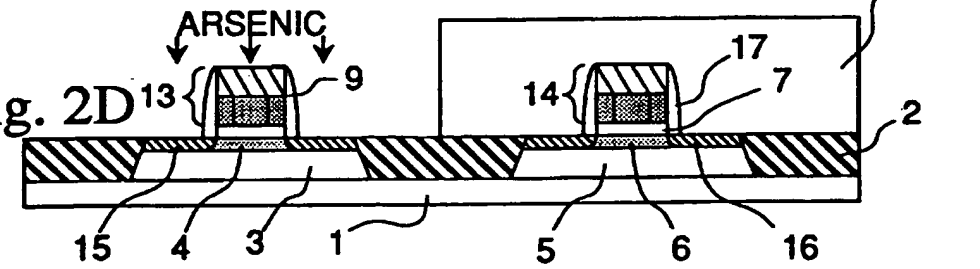



Fig. 2E

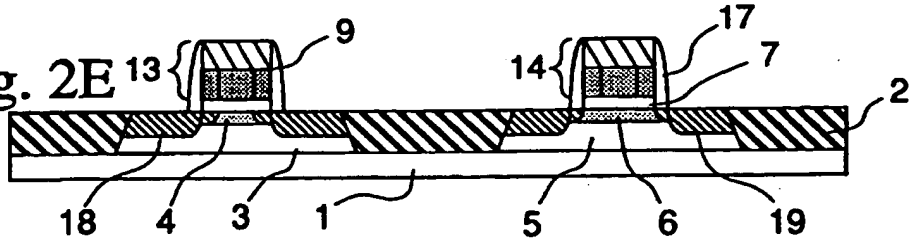



Fig. 2F

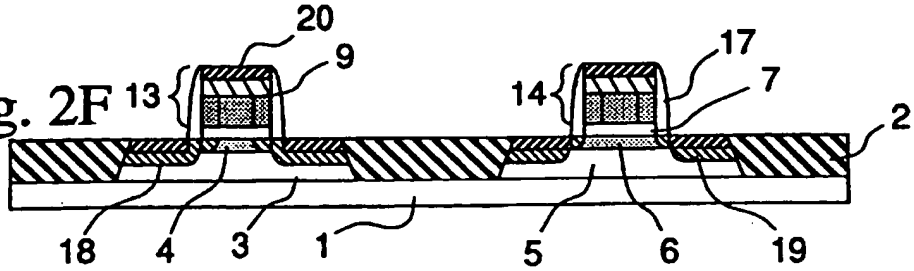


Fig. 6A

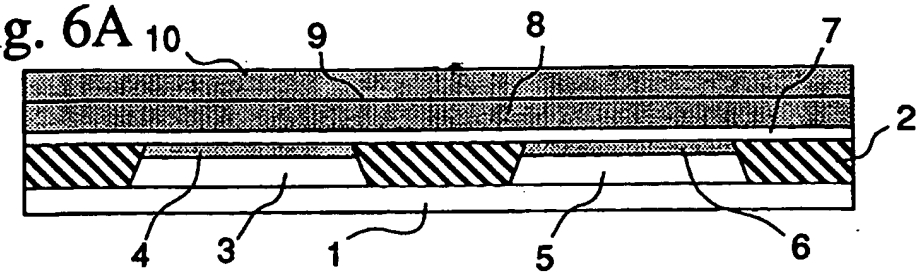



Fig. 6B

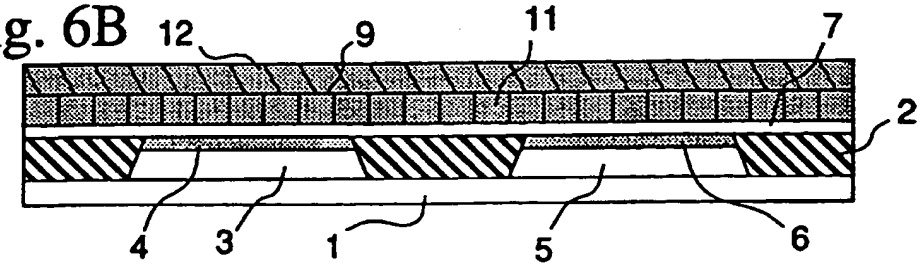



Fig. 6C

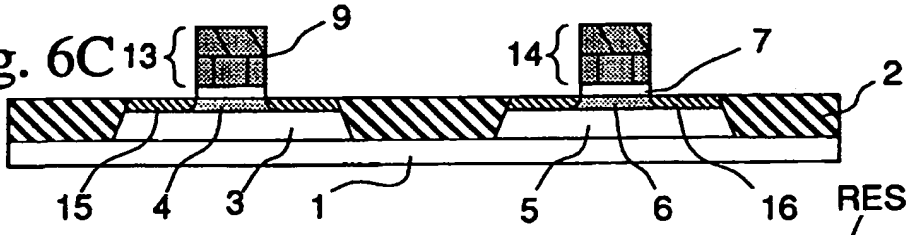



Fig. 6D

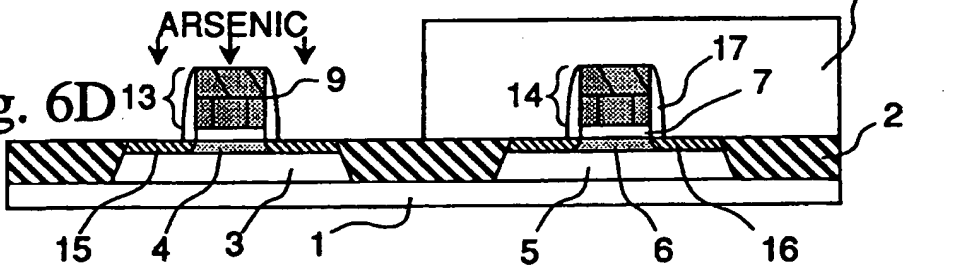



Fig. 6E

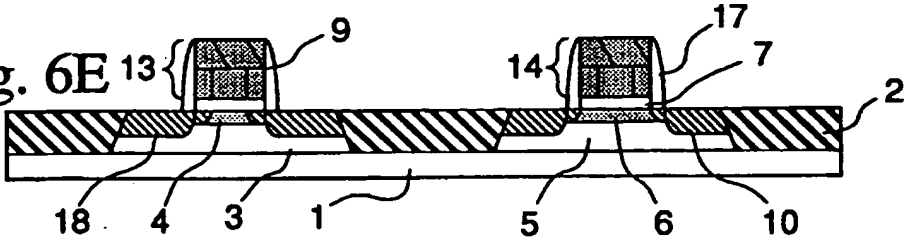
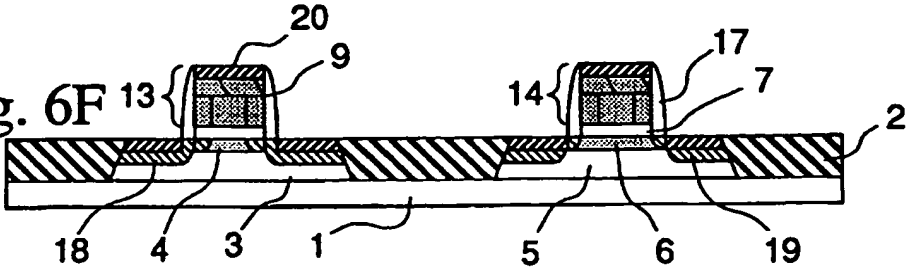



Fig. 6F



# SEMICONDUCTOR DEVICE AND METHOD OF MAKING THE SAME

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a semiconductor device having a gate electrode formed by a multi-layered structure and a method of making the same.

The present Application is based on Patent Application No. Hei 10-109208 filed in Japan, the content of which is incorporated herein by reference.

### Background Art

Recently, dual gate electrodes have been used for MOS transistors, that is, $N^+$ gates have been used for NMOS transistors and $P^+$ gates have been used for PMOS transistors.

In the case of using the dual gate structure, the following problems are encountered. One problem is that impurities can pass through the gate.

Practically, it is known that boron used as a dopant for the source/drain and the gate electrode passes from the gate electrode to the gate oxide layer and reaches the threshold control region (channel region) as a result of thermal treatment at high temperatures, which results in causing the

fluctuations of the threshold value.

This phenomenon is particularly remarkable when the boron is doped using boron fluoride ($BF_2$) by ion implantation.

Another problem is that the gate electrode is subjected to depletion. Actually, arsenic used for doping in the source/drain and the gate electrode is less thermally diffusible in comparison with boron. Thus, if the sufficient thermal treatment is not conducted after ion implantation of arsenic, the concentration of arsenic at the bottom surface of the NMOS-type gate electrode (near the interface with a gate oxide film) becomes low, causing depletion and reduction of the drain current.

The above mentioned two problems are opposite from the technical point of view and cannot be solved only by optimization of the heat treatment.

Moreover, it becomes an important object to improve the reliability of the gate oxide film, because the gate oxide film has become thinner with advances in the microstructure of transistors.

Recently, M. Koba et al. reported in "Improving Gate Oxide Integrity in p+ PMOSFET by Using Large Grain Size Polysilicon Gate" IEDM Tech. Dig., p. 471, 1993, that the initial withstanding voltage can be improved when the gate electrode is formed using large grain polycrystalline silicone.

However, H. Ito et al. reported in "Gate Electrode Microstructure Having Stacked Large-Grain Poly Si with Ultra-Thin SiOx Interlayer for Reliability in Sub-micrometer CMOS" IEDM Tech. Dig., p. 635, 1997, that, when a large grain polycrystalline silicon is used, the arsenic ion is likely to

cause channeling at the time of ion implantation of the arsenic for doping in the source/drain of NMOS and the gate electrode.

Consequently, it was discovered that the arsenic ion, which must remain in the gate electrode, reaches the surface of the silicon substrate and causes anomalies in the electric characteristics of the transistor.

In order to solve the above problem, H. Ito proposes a gate structure which is formed by double layers of the large grain polycrystalline silicon.

This gate structure is formed by inserting an electrically non-conductive oxide layer between two polycrystalline silicon layers such that the face orientation of the upper layer made of large grain polycrystalline silicon is not affected by the face orientation of the lower layer of large grain polycrystalline silicon.

The above structure including the oxide layer reduces the probability of channeling by the arsenic ion, because the face orientations of the upper and lower large grain polycrystalline silicon layers slip to each other.

Furthermore, by addition of an N-type phosphorous impurity at the concentration of $3 \times 10^{19}$ $cm^{-3}$ to those large grain polycrystalline silicon layers, a successful result is obtained in preventing depletion of the NMOS electrode, if the thermal treatment is performed within a temperature range in which the boron in the NMOS electrode does not pass through. As a result of this structure, two problems in the case of the dual gate structure can be settled.

A method is described below for manufacturing the dual gate CMOS proposed by H. Ito et al., which uses two layers of phosphorous doped large

grain polycrystalline silicon by placing one upon another.

As shown in Fig. 6A, element separating regions 2 are formed on a silicon substrate 1, a P well 3 and an NMOS channel region 4 are formed in the NMOS forming region, and an N well 5 and a PMOS channel region 6 are formed in the PMOS forming region.

After growing the gate oxide film 7, a first phosphorous doped amorphous silicon layer 8 is grown, and on that layer, an oxide layer 9 having a thickness of 1 $\mu$m is continuously grown by the use of a mixed gas of oxygen and nitrogen, and a second phosphorous doped amorphous silicon layer 10 is formed on the oxide layer 9. Here, the first and second phosphorous doped amorphous silicone layers 8 and 10 contain phosphorous at a concentration of $3 \times 10^{19}$ $cm^{-3}$.

Subsequently, as shown in Fig. 6B, a heat treatment is conducted (at 900℃ for 10 seconds) for crystallization of the first and the second phosphorous doped amorphous silicon layers 8 and 9, and a first phosphorous-doped large grain polysilicon layer 11 and a second phosphorous doped large grain polysilicon layer 12 are formed.

Subsequently, as shown in Fig. 6C, the NMOS gate electrode 13 and the PMOS gate electrode 14 are formed by patterning the first and second phosphorous-doped large grain polysilicon layers 11 and 12.

Next, an N-type LDD region 15 is formed by implanting phosphorous or arsenic in the NMOS region and a P-type LDD region is formed by implanting boron or $BF_2$ in the PMOS region.

As shown in Fig. 6D, after forming the side wall spacer 17, arsenic is implanted in the NMOS region to dope source/drain region 18 and the NMOS gate electrode into $N^+$.

Similarly, boron or $BF_2$ is implanted in the PMOS region to dope the source/drain region and PMOS gate electrode with $P^+$. At this time, the PMOS gate electrode 14 becomes $P^+$ by compensation of N-type dopants.

Next, as shown in Fig. 6E, the device is heat treated (at 1020℃ for 40 seconds) for activation.

As shown in Fig. 6F, silicide layers 20 are formed on the surfaces of the $N^+$ type source/drain region and NMOS gate electrode, and on the surfaces of the $P^+$ type source/drain region and the PMOS gate electrode in order to reduce the layer resistance.

The method of manufacturing the semiconductor device shown in Fig. 6 uses a gate electrode structure which is formed by double layers of phosphorous doped large grain polysilicon and the phosphorous at a concentration of $3 \times 10^{19}$ $cm^{-3}$ is contained as an impurity in the $P^+$ type PMOS electrode 14.

This impurity is introduced for preventing the depletion of the NMOS electrode 13, and the impurity of phosphorous in the PMOS electrode 14 is not substantially necessary. The N-type impurity of phosphorous is compensated by a P-type impurity of born in the source/drain region 19 and the gate electrode 14 of the PMOS.

However, there is a problem that the layer resistance of the PMOS gate

rises due to the presence of the phosphorous.

When the silicide layer is formed on the gate electrode surface, another problem arises that the contact resistance between the silicide layer and the large grain polysilicon forming the $P^+$ type gate electrode 14 rises.

Furthermore, since the upper and lower layers of large grain polysilicon have the same grain size, and if the upper layer and the lower layer are formed such that both layers have the same face orientation by chance, a problem arises that channeling of arsenic is caused.

It is therefore an object of the present invention to provide a semiconductor device and a method of producing the same in which the above problems are solved.

## SUMMARY OF THE INVENTION

A first aspect of the present invention provides a semiconductor device having a gate electrode formed in a multiple layered structure, wherein the bottom layer of the gate electrode is doped with an impurity.

By "bottom" we mean the layer which is closest to the substrate.

The impurity may be phosphorous as an N-type impurity.

The gate electrode may comprise multiple polycrystalline silicon layer and oxide layers which are not electrically conductive and which are inserted between said polycrystalline silicon layers.

The gate electrode may comprise polycrystalline silicon layers and the crystal grain size of the upper layers may be smaller than the crystal grain size of the lowermost polycrystalline silicon layer.

A second aspect of the present invention provides a method of manufacturing a semiconductor device having a multiple layered gate electrode;

wherein said method comprises the steps of:

growing an amorphous silicon layer containing a phosphorous dopant;

growing an oxide layer on said layer;

growing a non-doped amorphous silicon layer on said oxide layer; and

annealing to promote crystallization.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred features of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:-

Fig. 1 shows a cross sectional view of a semiconductor device according to an embodiment of the present invention.

Figs. 2A, 2B,,2C, 2D, 2E, and 2F are cross sectional views showing a method of manufacturing a semiconductor device of the present invention in the order of manufacturing processes.

Fig. 3 is a diagram showing a modified example of a semiconductor device according to the first embodiment of the present invention.

Fig. 4 is a diagram showing a modified example of a semiconductor device according to the second embodiment of the present invention.

Fig. 5 is a diagram showing a conventional semiconductor device.

Figs. 6A, 6B, 6C, 6D, 6E, and 6F are cross sectional views showing a method of manufacturing a conventional semiconductor device in the order of manufacturing process.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will be described with reference to the attached drawings.

[First Embodiment]

Fig. 1 shows a cross sectional view of a semiconductor device according to an embodiment of the present invention.

In Fig. 1, the semiconductor device according to an embodiment of the present invention comprises a gate electrode G formed by a multiple layered structure, wherein an impurity is only contained in the lowermost layer of the gate electrode G. The impurity is phosphorous as the N-type impurity.

The gate electrode G is composed of multiple layers of polycrystalline silicon layers 23 and 24, and a non-conductive oxide layer 9 is inserted between polycrystalline silicon layers 23 and 24.

The gate electrode G is composed of multiple layers 23 and 24 of polysilicon and the grain size of the upper polycrystalline silicon layer 24 is smaller than that of the lowermost polycrystalline silicon layer 23.

As shown in Fig. 5, in a conventional gate electrode formed by multi-layered large grain polysilicone, all of the stacked polysilicone multiple layers 11, 11 are doped with phosphorous. However, in the gate electrode according to first embodiment of the present invention shown in Fig. 1, only the lowermost large grain size polysilicon layer 23 is doped with phosphorous.

Consequently, according to the first embodiment of the present invention, since the upper polysilicone layer is not doped with phosphorous, the polycrystalline silicone layer is capable of, while playing a role to suppressing the depletion of the gate electrode of the NMOS, restricting the increase of the layer resistance of the PMOS gate electrode and preventing an increase of the contact resistance between the silicide layer formed on the gate electrode.

According to the first embodiment of the present invention, the large grain size silicone layer 23 is formed by crystallization of the annealed amorphous silicone layer.

It is known that the crystal grain size becomes large in the annealing and crystallizing processes, if the amorphous silicone layer includes an impurity.

In the conventional example shown in Fig. 4, since all of the layers 25, 25 are doped with phosphorous, the grain sizes of the large grain polycrystalline silicon layers 25, 25 are the same.

In contrast, in the first embodiment of the present invention shown in Fig. 1, only the lowermost layer 13 is doped with phosphorous to be converted

into a large grain polycrystalline silicon layer, and the upper layer not containing the dopant of phosphorous is formed with smaller grain size than that of the lowermost layer 24.

The polycrystalline silicon layer with a comparatively smaller crystal size is effective in preventing channeling. Therefore, the first embodiment of the present invention, while maintaining the initial withstanding voltage of the gate oxide film 7, is more capable of suppressing the channeling of arsenic than the conventional method.

Hereinafter, the method of manufacturing the semiconductor device according to the first embodiment of the present invention is described in the order of processing.

As shown in Fig. 2A, an element separating region 2 is formed on the silicon substrate 1, a P well 3 and a NMOS channel region 4 are formed in the NMOS forming region, and N well 5 and a PMOS channel region 6 are formed in the PMOS forming region.

After growing a gate oxide layer 7, a phosphorous doped amorphous silicon layer 8 containing phosphorous at a concentration of $3 \times 10^{19}$ $cm^{-3}$ is grown, an oxide layer 9 is grown continuously on the amorphous silicon layer by a mixture of oxygen and nitrogen, and a non-doped amorphous silicon layer 22 is further grown thereon.

As shown in Fig. 2B, a heat treatment (at 900℃ for 10 seconds) is executed for crystallization of the phosphorous doped amorphous silicone layer 8 and the non-doped amorphous silicone layer 22 to form a phosphorous

doped large grain polycrystalline silicon layer 11 and a non-doped polycrystalline silicon layer 23. Since the non-doped polycrystalline silicon layer 23 does not includes phosphorous, the crystal grain size of this non-doped polycrystalline silicon layer is smaller than that of the phophorous doped polycrystalline silicon layer 11.

Next, as shown in Fig. 2C, the NMOS gate electrode 13 and the PMOS gate electrode 14 are formed by patterning the phosphorous doped large grain polycrystalline silicon 11 and the non-doped polycrystalline silicone layer 23.

Thereafter, an N-type LDD 15 is formed by implanting phosporous or arsenic in the NMOS region, and a P-type LDD is formed by implanting boron or $BF_2$.

Next, as shown in Fig. 2D, implanting arsenic in the NMOS region is carried out after forming the side wall spacer 17 for doping the source/drain region 18 and the NMOS gate electrode 13 into $N^+$. Similarly, implanting boron or $BF_2$ in the PMOS region is carried out for doping the source/drain region 19 and the PMOS gate electrode 14 into $P^+$.

Next, as shown in Fig. 2E, the heat treatment for activation (at 1020℃ for 40 seconds) is executed.

Next, as shown in Fig. 2F, silicide layers 20 are formed on the surfaces of the $N^+$ type source/drain region 18, NMOS gate 13, P+ type source/drain region 19, and PMOS gate 14.

As shown in Figs. 1 and 2, according to the first embodiment of the present invention, in the gate electrode which is formed of two or more than

two layers of polycrystalline layers, the lowermost layer of the gate electrode is doped with an N-type impurity of phosphorous and is comprised of a large grain polycrystalline silicon layer 23, and the upper layer 24 on the lowermost silicon layer does not contain an impurity of posphorous.

Therefore, while the lowermost layer 23, which includes phosphorous and which is formed of a large grain polycrystalline silicone layer, plays a role to suppress the depletion of nMOD similar to the conventional role, the upper layer, which does not include phosphorous, is capable of preventing an increase of the layer resistance of the PMOS gate electrode 14 and preventing contact resistance with the silicide layer 20.

In addition, the grain size of the upper polycrystalline silicon layer 24 is smaller than that of the lowermost large grain polycrystalline silicon layer 23. The large grain sized polycrystalline silicon layer is produced by annealing and crystallizing the amorphous silicon layer. It is known that, if the amorphous silicon layer includes an impurity, the crystal grain size becomes larger.

In the conventional example shown in Fig. 5, all of the layers forming the gate electrode are doped with phosphorous, so that the grain size of every large grain polycrystalline silicon layer 11, 11 is the same.

In contrast, in the first embodiment of the present invention shown in Figs. 1 and 2, the lowermost layer 23 containing phosphorous only is composed of larger grains, and upper layer 24 which does not contain the phosphorous dopant is formed of small grain polycrystalline silicon.

The polycrystalline silicon layer composed of small grains is effective in suppressing channeling by the arsenic dopant. Therefore, the first embodiment of the present invention, while preserving the initial withstanding voltage of the gate oxide layer as usual, is effective in suppressing the arsenic channeling.

In the first embodiment of the present invention shown in Fig. 1, an example is described which has one layer of the non-dope polycrystalline silicon. However, it is possible to produce a semiconductor device with two or more than two layers of the non-doped polycrystalline layers 24 as shown in Fig. 3, which is more preferable because of it is more capable of effectively preventing the channeling.

[Second Embodiment]

Fig. 4 shows a cross sectional view of the second embodiment of the present invention.

The second embodiment of the present invention is, as shown in Fig. 4, used for a semiconductor device having a gate electrode G composed of three or more than three layers of polycrystalline silicon layers. The lowermost layer is formed by a large grain polycrystalline silicon layer 23 containing an n-type impurity of phosphorous, wherein upper polycrystalline silicone layers 24 do not contain the phosphorous dopant, and the grain size of the upper polycrystalline silicon layers 24 is smaller than that of the lowermost large size polysilicon layer.

In the second embodiment of the present invention shown in Fig.4, the

grain size of the upper polycrystalline layers is made far smaller than the grain size of the lowermost polycrystalline layer by decreasing the height of the crystal grains in the upper layers than the height of the crystal grains of the lowermost layer. This is practically realized by reducing the intervals of inserting the oxide film between polycrystalline silicon layers 24, as opposed to disposing the oxide films 9 at the same interval.

As hereinabove described, the gate electrode of the present invention is formed by a multiple layered structure, in which only the lowermost layer is doped with an impurity as a dopant, and upper layers are formed as non-doped layers. Therefore, the gate electrode of the present invention suppresses the depletion of the gate electrode as usual, suppresses the layer resistance of the gate electrode, and prevents the resistance of the silicide layer formed on the gate electrode surface from increasing.

Furthermore, since the lowermost layer only is crystallized into larger crystal grains, and the upper layers are crystallized into smaller crystal grains, and because the upper layers do not include an impurity, the gate electrode of the present invention is capable of reducing the channeling to a smaller level than usual, while improving the initial withstanding voltage of the oxide layer.

Each feature disclosed in this specification (which term includes the claims) and/or shown in the drawings may be incorporated in the invention independently of other disclosed and/or illustrated features.

Statements in this specification of the "objects of the invention" relate to preferred embodiments of the invention, but not necessarily to all embodiments of the invention falling within the claims.

The description of the invention with reference to the drawings is by way of example only.

The text of the abstract filed herewith is repeated here as part of the specification.

A semiconductor device is provided which is capable of suppressing an increase in the layer resistance of the gate electrode and preventing an increase of the contact resistance of the gate electrode with the silicide layer.

The above properties of the semiconductor device are provided by forming the gate electrode comprising multiple layers, and the lowermost layer of the gate electrode is doped with an impurity, and other upper layers are formed undoped.

**CLAIMS**:

1. A semiconductor device having a gate electrode formed in a multiple layered structure, wherein the bottom layer of the gate electrode is doped with an impurity.

2. A semiconductor device according to Claim 1, wherein said impurity is phosphorous as an N-type impurity.

3. A semiconductor device according to Claim 1 or 2, wherein said gate electrode comprises multiple polycrystalline silicon layers and oxide layers between said polysilicon layers and which are not electrically conductive.

4. A semiconductor device according to any preceding claim, wherein said gate electrode comprises polycrystalline silicon layers and the crystal grain size of the upper layers of the gate electrode is smaller than the crystal grain size of the bottom polycrystalline silicon layer.

5. A method of manufacturing a semiconductor device having a multiple layered gate electrode; wherein said method comprises the steps of:

growing an amorphous silicon layer containing a phosphorous dopant;

growing an oxide layer on said layer;

growing a non-doped amorphous silicon layer on said oxide layer; and annealing to promote crystallization.

6. A semiconductor device substantially as herein described with reference to any of Figures 1, 3 and 4 of the accompanying drawings.

7. A method of manufacturing a semiconductor device substantially as herein described with reference to Figures 2A to 2F of the accompanying drawings.

The Patent Office

INVESTOR IN PEOPLE

**Application No:** GB 9908779.3 **Examiner:** Martyn Dixon
**Claims searched:** all **Date of search:** 15 July 1999

# Patents Act 1977
# Search Report under Section 17

**Databases searched:**

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.Q): H1K (KCAA,KCAL,KCAX,KGAFX,KGAGX,KHAAX,KHABP, KHAC,KHAX)

Int Cl (Ed.6): H01L

Other: Online: EPODOC,WPI,JAPIO

**Documents considered to be relevant:**

| Category | Identity of document and relevant passage | | Relevant to claims |
|---|---|---|---|
| X,P | GB 2318451 A | (NEC) see e.g. fig 3, page 12, line 26 to page 15, line 17 and page 19, lines 10-18 | 1-3 |
| X | GB 2300298 A | (Hyundai) see page 5, line 26 to page 6, line 6 | 1,2,4 |
| X | GB 2254960 A | (Samsung) the whole document | 1,2,4 |
| X | EP 0497596 A | (SGS-Thomson) see col 3, lines 13-33 | 1,2 |
| X | EP 0466166 A | (Toshiba) the whole document | 1,2 |
| X | EP 0364818 A | (Motorola) see col 4, lines 34-38 | 1,3 |
| X | US 5652156 A | (Taiwan Semiconductor) see figs 7,8 | 1,2 |
| X,A | JP 010093077 A | (Sony) see abstract | X:1,2 A:5 |

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| X | Document indicating lack of novelty or inventive step | A | Document indicating technological background and/or state of the art. |
| Y | Document indicating lack of inventive step if combined with one or more other documents of same category. | P | Document published on or after the declared priority date but before the filing date of this invention. |
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